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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,350	09/26/2001	Tomaas Jackson	PD-200293	8267

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,350	JACKSON ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/01/02; 09/26/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,4-7,10-13 and 16-18* is/are rejected.

7)☒ Claim(s) *2,3,8,9,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/1/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated as cited in paragraph 003 in the specification. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4-7, 10-13, and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by the admitted prior art.

Re claim 1, the admitted prior art discloses in Figures 1 and 2 a sigma delta interpolator for use in a fractional N synthesizer (Figure 1) having a multi-modulus divider, sigma delta interpolator comprising: an accumulator (21) operative for receiving

an input signal (Input n-BITS in Figure 2) representing a desired frequency output of fractional N synthesizer and for generating a digital output signal having M bits (output of 25 in Figure 2), which include N most significant bits (27) and n least significant bits (input to 26), N most significant bits being coupled to multi-modulus divider (Figure 1) and operative for controlling the operation of multi-modulus divider (20 in Figure 1); and a delay circuit (26) coupled to accumulator (25), delay circuit (25) receiving n least significant bits (input into 26 in Figure 2) and operative for implementing a delay function defined by equation: $1-(1-Z^{-1})^N$ wherein N corresponds to the order of the sigma delta interpolator (wherein N = 1).

Re claim 4, the admitted prior art further discloses in Figures 1 and 2 the N most significant bits output by accumulator correspond to desired frequency output of fractional N synthesizer (Figure 2).

Re claim 5, the admitted prior art further discloses in Figures 1 and 2 the accumulator is the sole accumulator utilized in sigma delta interpolator (Figure 2).

Re claim 6, the admitted prior art further discloses in Figures 1 and 2 the N most significant bits output by accumulator and coupled to multi-modulus divider are the sole control signals received by multi- modulus divider the effect the desired output frequency generated by fractional N synthesizer (Figure 1).

Re claim 7, it has means limitations cited in claim 1. Thus, claim 7 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 10, it has means limitations cited in claim 4. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 11, it has means limitations cited in claim 5. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 12, it has means limitations cited in claim 6. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 13, it has the same limitations cited in claim 1. In addition, the admitted prior art further discloses in Figures 1-2 a phase-lock loop circuit (14) comprising a voltage controlled oscillator (18) for generating a carrier signal and a programmable frequency divider (20), programmable frequency divider(20) receiving N most significant bits as an input signal (output of 21), programmable frequency divider (20) operative for changing the frequency of the carrier signal in accordance with N most significant bits,

Re claim 16, it has same limitations cited in claim 4. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 17, it has same limitations cited in claim 5. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 18, it has same limitations cited in claim 6. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Allowable Subject Matter

4. Claims 2-3, 8-9, and 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,270,026 to Shenoi et al. disclose an interpolator apparatus for increasing the word rate of a digital signal of the type employed in digital telephone systems.

b. U.S. Patent No. 4,302,631 to Shenoi et al. disclose a decimator apparatus for decreasing the word rate of a digital signal of the type employed in digital telephone systems.

c. U.S. Patent No. 5,786,778 to Adams et al. disclose a variable sample-rate DAC/ADC/converter sytem.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

August 23, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100